What is claimed is:

1. A method for producing a photomask for semiconductor photolithography processing comprising:

for each pitch of a plurality of pitches within a semiconductor design, determining a bias needed at the pitch that maximizes a common process window for the plurality of pitches given a critical dimension (CD) specification for a semiconductor design of the photomask;

modifying an original layout for the semiconductor design of the photomask by performing rule-based optical-proximity correction (OPC), including adding the bias determined at each pitch, to yield a modified layout for the semiconductor design of the photomask; and,

further modifying the modified layout for the semiconductor design of the photomask by performing model-based on the modified layout such that exposed semiconductor wafer CD's at each pitch are at least substantially equal to the CD specification for the pitch, to yield a final layout for the semiconductor design of the photomask.

2. The method of claim 1, wherein determining the bias needed comprises determining the bias needed by simulation.

3. The method of claim 1, wherein determining the bias needed comprises determining the bias needed by experiment.

4. The method of claim 1, wherein modifying the original layout for the semiconductor design of the photomask by adding the bias determined at each pitch comprises retargeting the CD's of the original layout.

5. The method of claim 1, wherein the common process window has a first axis measuring depth of focus (DOF) and a second axis measuring light-exposure dose.

6. The method of claim 5, wherein the first axis is an x-axis and the second axis is a y-axis.

7. A photomask for semiconductor photolithography processing comprising:

a semiconductor design having a critical dimension (CD) specification and having had applied thereto rule-based and model-based optical proximity correction (OPC), the rule-based OPC including application of biases determined at each of a plurality of pitches of the semiconductor design;

a plurality of pitches within the semiconductor design; and,

a maximized common process window for the plurality of pitches given the CD specification.

8. The photomask of claim 7, wherein the common process window has a first axis measuring depth of focus (DOF) and a second axis measuring light-exposure dose.

9. The photomask of claim 8, wherein the first axis is an x-axis and the second axis is a y-axis.

10. The photomask of claim 7, wherein the maximized common process window is determined by determining a bias needed at each pitch that maximizes the common process window, and adding the bias determined at each pitch.

11. The photomask of claim 10, wherein the maximized common process window is further determined by performing rule-based and model-based OPC such that exposed semiconductor wafer CD's at each pitch are at least substantially equal to the CD specification for the pitch.

12. The photomask of claim 10, wherein determining the bias needed at each pitch comprises determining the bias needed at each pitch by simulation.

13. The photomask of claim 10, wherein determining the bias needed at each pitch comprises determining the bias needed at each pitch by experiment.

14. A semiconductor device formed at least in part by a method comprising:

positioning a photomask over a semiconductor wafer having a top layer of photoresist, the photomask having a maximized common process window for a plurality of pitches of a semiconductor design to which rule-based and model-based optical proximity correction (OPC) has been applied, given a critical dimension (CD) specification of the semiconductor design, the rule-based OPC including application of biases determined at each of a plurality of pitches of the semiconductor design;

exposing the semiconductor wafer through the photomask positioned thereover, such that the top layer of photoresist includes exposed parts under clear parts of the photomask and unexposed parts under opaque parts of the photomask;

developing the semiconductor wafer to remove the exposed parts of the top layer of photoresist;

etching the semiconductor wafer where the wafer is revealed through the exposed parts of the top layer of photoresist that has been removed; and,

removing the unexposed parts of the top layer of photoresist.

15. The semiconductor device of claim 14, wherein the common process window has a first axis measuring depth of focus (DOF) and a second axis measuring light-exposure dose.

16. The semiconductor device of claim 15, wherein the first axis is an x-axis and the second axis is a y-axis.

17. The semiconductor device of claim 14, wherein the maximized common process window is determined by determining a bias needed at each pitch that maximizes the common process window, and adding the bias determined at each pitch.

18. The semiconductor device of claim 17, wherein the maximized common process window is further determined by performing rule-based and model-based OPC such that exposed semiconductor wafer CD's at each pitch are at least substantially equal to the CD specification for the pitch.

19. The semiconductor device of claim 17, wherein determining the bias needed at each comprise comprises determining the bias needed at each pitch by simulation.

20. The semiconductor device of claim 17, wherein determining the bias needed at each comprise comprises determining the bias needed at each pitch by experiment.